1. A system wherein data is read from, and store in, a memory, such data having associated therewith an address/control portion, such system comprising:

(A) a pair of controller sections, one of such sections being a primary section and the other one of the sections being a secondary section, both such sections being configured to implement identical control logic in controlling the transfer of such data between a first port connected to the pair of control sections and a write data port, the write data port of the primary section being connected to the memory, such first port receiving an address/control portion associated with the data; and

(B) a checker producing a NOOP command to the memory if logic signal produced by the pair of control logic from the address/control portion at the first port are different from one another.

2. The system recited in claim 1 wherein the memory is configured to inhibit storage of data in the memory at the data port in response to the NOOP command.

3. A system wherein data is read from, and store in, a memory, such data having associated therewith an address/control portion, such system comprising:

(A) a pair of controller sections, one of such sections being a primary section and the other one of the sections being a secondary section, both such sections being configured to implement identical control logic in controlling the transfer of such data between a first port connected to the pair of control sections and a write data port of the primary section, the write data port of the primary section being connected to the memory, such first port receiving the address/control portion associated with the data; and

(B) a checker producing a NOOP command to the memory if a parity bit generated by a first parity generator in the primary section from the address/control portion at the first port and a parity bit generated by the first parity generator of the secondary section from the address/control portion at the first port are the same, or different.

4. The system recited in claim 3 wherein the memory is configured to inhibit storage of data at the data port in the memory in response to the NOOP command.

5. A system wherein data is read from, and store in, a memory, such data having associated therewith an address/control portion, such system comprising:

(A) a pair of controller sections, one of such sections being a primary section and the other one of the sections being a secondary section, both such sections being configured to implement identical control logic in controlling the transfer of such data between a first port connected to the pair of control sections and a write data port of the primary section, such write data port of the primary section being connected to the memory, such first port receiving the address/control portion associated with the data; and

(B) a checker producing a NOOP command to the memory if the digital word generated by a first parity generator of primary section from the address/control portion at the first port and the digital word generated by a first parity generator of secondary section from the address/control portion at the first port are the same or different.

6. The system recited in claim 5 wherein the memory is configured to inhibit storage of data at the data port in the memory in response to the NOOP command.

7. A system wherein data is read from, and store in, a memory, such data having associated therewith an address/control portion, such system comprising:

(A) a pair of controller sections, one of such sections being a primary section and the other one of the sections being a secondary section, both such sections being configured to implement identical control logic in controlling the transfer such data between a first port connected to the pair of control sections and a write data port of the primary section, such write data port of the primary section being connected to the memory, such first port receiving the address/control portion associated with the data; and

(B) a checker producing a NOOP command to the memory if a parity bit generated by a first parity generator in the primary section the address/control portion at the first port and a parity bit generated by the first parity generator of the secondary section from the address/control portion at the first port are the same, or different, or if a digital word generated by the first parity generator of primary section a digital word generated by the first parity generator of secondary section from the address/control portion at the port are the same or different.

8. The system recited in claim 7 wherein the memory is configured to inhibit storage of data in the memory at the data port in response to the NOOP command.

9. A system wherein data is read from, and store in, a memory, such data having associated therewith an address/control portion, such system comprising:

(A) a pair of controller sections, one of such sections being a primary section and the other one of the sections being a secondary section, both such sections being connected to a first port, both such sections being configured to implement identical control logic in controlling the transfer such data between the first port and the write data port, each one of the sections, comprising:

a first parity generator coupled to the first port; for generating a parity bit for an address/control digital word, such digital word comprising the address/control portion associated with the data at such first port;

(B) a checker, comprising:

a second parity generator for generating a parity bit from the digital word and for passing there-through to an address/control port either:

the parity bit generated by the second parity generator or,

an inverted parity bit of the parity bit generated by the second parity bit generator, selectively in accordance with:

whether the parity bit generated by the first parity generator in the primary section and the parity bit generated by the first parity generator of the secondary section are the same, or different, or if the digital word generated by the first parity generator of primary section and the digital word generated by the first parity generator of secondary section are the same or different.

10. The system recited in claim 9 wherein the memory is configured to inhibit storage of data at the data port in the memory if either:

the inverted parity bit of the inverter is passed through the selector to the address/control port because either the parity bit generated by the first parity generator in the primary section and the parity bit generated by the first parity generator of the secondary section are different; or

the digital word generated by the first parity generator of primary section and the digital word generated by the first parity generator of secondary section are different.

11. A system wherein data is read from, and store in, a memory, such data having associated therewith an address/control portion, such system comprising:

a controller having:

(A) a first port:

for receiving data to be stored in the memory; and

for receiving the address/control portion associated with such data;

(B) an address/control port connected to the memory for transmitting address and memory read/write control signals to the memory;

(C) a write data port connected to the memory for transmitting data to be stored in the memory;

(D) a pair of controller sections, one of such sections being a primary section and the other one of the sections being a secondary section, both such sections being connected to the first port, both such sections being configured to implement identical control logic in controlling the transfer such data between the first port and the write data port, each one of the sections, comprising:

a first parity generator coupled to the first port; for generating a parity bit for an address/control digital word, such digital word comprising the address/control portion associated with the data at such first port;

(E) a checker, comprising:

a second parity generator for generating a parity bit from the digital word and for passing there-through to an address/control port either:

the parity bit generated by the second parity checker; or,

the inverted parity bit of the inverter, selectively in accordance with:

whether the parity bit generated by the first parity generator in the primary section and the parity bit generated by the first parity generator of the secondary section are the same, or different, or if the digital word generated by the first parity generator of primary section

and the digital word generated by the first parity generator of secondary section are the same or different.

12. The system recited in claim 11 wherein the memory is configured to inhibit storage of data at the data port in the memory if either:

the inverted parity bit of the inverter is passed through the selector to the address/control port because either the parity bit generated by the first parity generator in the primary section and the parity bit generated by the first parity generator of the secondary section are different; or

the digital word generated by the first parity generator of primary section and the digital word generated by the first parity generator of secondary section are different.

13. A system wherein data is read from, and store in, a memory, such data having associated therewith an address/control portion, such system comprising:

a controller having:

(A) a first port:

for receiving data to be stored in the memory and for transmitting data read from the memory; and

for receiving the address/control portion associated with such data;

(B) an address/control port connected to the memory for transmitting address and memory read/write control signals to the memory to the controller;

(C) a read data port connected to the memory for receiving data read from the memory;

(D) a write data port connected to the memory for transmitting data to be stored in the memory;

(E) a pair of controller sections, one of such sections being a primary section and the other one of the sections being a secondary section, both such sections being connected to the first port, both such sections being configured to implement identical control logic in controlling the transfer such data between the first port and the read and write data ports, each one of the sections, comprising:

a first parity generator coupled to the first port; for generating a parity bit for an address/control digital word, such digital word comprising the address/control portion associated with the data at such first port;

(F) a checker, comprising:

(a) a second parity generator for generating a parity bit for the address/control digital word generated by the primary section;

(b) an inverter for inverting the parity bit generated by the second parity bit generator;

(c) a selector for passing there-through to the address/control port either:

the parity bit generated by the second parity checker; or,

the inverted parity bit of the inverter, selectively in accordance with:

whether the parity bit generated by the first parity generator in the primary section and the parity bit generated by the first parity generator of the secondary section are the same, or different, or if the digital word generated by the first parity generator of primary section and the digital word generated by the first parity generator of secondary section are the same or different.

14. The system recited in claim 13 wherein the memory is configured to inhibit storage of data at the data port in the memory if either:

the inverted parity bit of the inverter is passed through the selector to the address/control port because either the parity bit generated by the first parity generator in the primary section and the parity bit generated by the first parity generator of the secondary section are different; or

the digital word generated by the first parity generator of primary section and the digital word generated by the first parity generator of secondary section are different.